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EXAMINER	
MIYOSHI, JESSE Y	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/564,486	SON, HYO-KUN	
	Examiner	Art Unit	
	JESSE Y. MIYOSHI	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *33,37-39,41,42,47-49,51,53 and 55-59* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *33,37-39,41,42,47-49,51,53 and 55-59* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 33, 37-39, 41, 51, 53, 54 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanizawa et al. (US PGPub 2003/0205711; hereinafter "Tanizawa") in view of Vaudo et al. (U.S. 6,440,823; hereinafter "Vaudo").

Re claim 33: Tanizawa teaches (e.g. figure 1) a light emitting diode (LED), comprising: a first gallium nitride layer (**5c**) having a first conductivity (n-type GaN; e.g. paragraph 57); a super lattice structure (multi-layered film **6** of $In_kGa_{1-k}N$/ $In_mGa_{1-m}N$ structure, where m<k; e.g. paragraph 64) including InGaN ($In_kGa_{1-k}N$/ $In_mGa_{1-m}N$) on the first gallium nitride layer (**5c**), wherein the super lattice structure (**6**) is not doped with an n-type impurity (to enhance crystallinity, both first and second nitride semiconductor layers are preferably undoped; e.g. paragraph 65), wherein the super lattice structure (**6**) includes a plurality of first InGaN layers ($In_kGa_{1-k}N$; hereinafter "**FL**") and a plurality of second InGaN layers ($In_mGa_{1-m}N$; hereinafter "**SL**"), wherein each of the plurality of first InGaN layers (**FL**) has an In composition less (m<k; e.g. paragraph 64) than an In composition of each of the plurality of second InGaN layers (**SL**), and wherein the first InGaN layer (**FL**) is directly on (as discussed at paragraph 63, the sequence of the layers comprising **6** may be arbitrarily chosen, therefore, the order can be **FL**, **SL**, **FL**,

SL or **SL**, **FL**, **SL**, **FL**, therefore, the first sequence would result in **FL** being directly on **5c**) the first gallium nitride layer (**5c**); an active layer (**7**) on the super lattice structure (**6**) and including an InGaN/InGaN structure (active layer **7** is a multiple quantum-well structure made from $In_aGa_{1-a}N$; e.g. paragraph 68) of a multi-quantum well structure (multiple quantum-well structure; e.g. paragraph 68), wherein the active layer (**7**) is directly on (as discussed at paragraph 63, the sequence of the layers comprising **6** may be arbitrarily chosen, therefore, the order can be **FL**, **SL**, **FL**, **SL** or **SL**, **FL**, **SL**, **FL**, therefore, the first sequence would result in **7** being directly on **SL**) one of the plurality of second InGaN layers (**SL**); and a second gallium nitride layer (p-type GaN; e.g. paragraph 77) having a second conductivity (p-type) on the active layer (**7**), wherein the super lattice structure (**6**) including InGaN has a plurality of pits formed thereon (number of pits occurring in each nitride semiconductor layer; e.g. paragraph 64).

Tanizawa is silent as to explicitly teaching wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm.

Vaudo teaches LED structure with reduced number of pits and further teaches and further teaches a non-zero number of the plurality of pits (base GaN has hexagonal pit density of approximately 10^6cm^{-2} and can be reduced to less than 50 pits per cm^2; e.g. column 16, lines 15-17) is 50 or less per area of 5μm x 5μm. Since 25 pits per μm^2 is approximately $2x10^8$ pits per cm^2, Vaudo's pit density of less than 50 pits per cm^2 meets said claim limitation because any subsequent nitride based layer will have the same, if not less, pits than the density of pits at the base GaN layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo in the device of Tanizawa and have a base GaN layer having less than 50 pits per cm2 allowing for a high quality epitaxial growth to be attained (see column 16, lines 29-30 of Vaudo) and since it is a goal of Tanizawa to decrease the number of pits, Vaudo's teachings would allow for high quality epitaxial layers with less pits to be grown.

Re claim 37: Tanizawa teaches the LED wherein the super lattice structure (**6**) including InGaN includes an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer is formed to have a super lattice structure (multi-layered film **6** of $In_kGa_{1-k}N/ In_mGa_{1-m}N$ structure; e.g. paragraph 64).

Re claim 38: Tanizawa teaches the LED wherein each layer of the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer ($In_kGa_{1-k}N/ In_mGa_{1-m}N$) has a thickness of 1-3000Å (100Å, 70Å; e.g. paragraph 62).

Re claim 39: Tanizawa teaches the LED, wherein the super lattice structure (**6**) including InGaN has a photoluminescence characteristic of a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below. Since the structure recited in the prior art is substantially identical to that of the claim, claimed properties are presumed to be present. See MPEP 2112.01(i).

Re claim 41: Vaudo teaches the LED wherein the LED is blue LED (UV to green light emitting diodes; e.g. column 1, line 36).

Re claim 51: Tanizawa teaches (e.g. figure 1) a light emitting diode (LED), comprising: a substrate (**1**); a buffer layer (**2**) on the substrate (**1**); an undoped GaN

layer (upper portion of **3**; hereinafter "**UDG**") on the buffer layer (**2**); a GaN layer (lower portion of **3**; hereinafter "**GL**") between the buffer layer (**2**) and the undoped GaN layer (**UDG**); an N-type GaN layer (**4**, **5**) directly on the undoped GaN layer (**UDG**); a super lattice structure (**6**) including InGaN ($In_kGa_{1-k}N$/ $In_mGa_{1-m}N$) directly on the N-type GaN layer (**4**, **5**), wherein the super lattice structure (**6**) is not doped (to enhance crystallinity, both first and second nitride semiconductor layers are preferably undoped; e.g. paragraph 65) with an n-type impurity, wherein the super lattice structure (**6**) including InGaN includes a plurality of first layers ($In_kGa_{1-k}N$; hereinafter "**FL**") and a plurality of second layers ($In_mGa_{1-m}N$; hereinafter "**SL**"), wherein each of the plurality of first layers (**FL**) has an In composition less than (m<k; e.g. paragraph 64) an In composition of each of the plurality of second layers (**SL**), wherein the first layer (**FL**) is directly on (as discussed at paragraph 63, the sequence of the layers comprising **6** may be arbitrarily chosen, therefore, the order can be **FL**, **SL**, **FL**, **SL** or **SL**, **FL**, **SL**, **FL**, therefore, the first sequence would result in **FL** being directly on **4, 5**) the N-type GaN layer (**4**, **5**), wherein each of the first layers (**FL**) has a thickness of 1-3000Å (100Å; e.g. paragraph 62), and wherein each of the second layers (**SL**) has a thickness of 1-3000Å (70Å; e.g. paragraph 62); an active layer (**7**) on the super lattice structure (**6**) including an InGaN/InGaN structure of a multi-quantum well structure (active layer **7** is a multiple quantum-well structure made from $In_aGa_{1-a}N$; e.g. paragraph 68), wherein the active layer (**7**) is directly on (as discussed at paragraph 63, the sequence of the layers comprising **6** may be arbitrarily chosen, therefore, the order can be **FL**, **SL**, **FL**, **SL** or **SL**, **FL**, **SL**, **FL**, therefore, the first sequence would result in **7** being directly on **SL**) the

second layer (**SL**); and a P-type GaN layer (p-type GaN; e.g. paragraph 77) on the active layer (**7**), wherein the super lattice structure (**6**) including InGaN has a plurality of pits thereon (number of pits occurring in each nitride semiconductor layer; e.g. paragraph 64).

Regarding the claim limitations of "a GaN layer between the buffer layer and the undoped GaN layer", these are inherent in the structure of Tanizawa (figure 1) for the following reasons. The structure of a GaN layer formed on an undoped GaN layer is indistinguishable from the structure comprising an undoped GaN layer. Therefore, the claim limitations of "a GaN layer between the buffer layer and the undoped GaN layer" are process limitations, which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Tanizawa is silent as to explicitly teaching wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm.

Vaudo teaches LED structure with reduced number of pits and further teaches and further teaches a non-zero number of the plurality of pits (base GaN has hexagonal pit density of approximately $10^6 cm^{-2}$ and can be reduced to less than 50 pits per cm^2; e.g. column 16, lines 15-17) is 50 or less per area of 5μm x 5μm. Since 25 pits per μm^2 is approximately $2x10^8$ pits per cm^2, Vaudo's pit density of less than 50 pits per cm^2 meets said claim limitation because any subsequent nitride based layer will have the same, if not less, pits than the density of pits at the base GaN layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo in the device of Tanizawa and have a base GaN layer having less than 50 pits per cm2 allowing for a high quality epitaxial growth to be attained (see column 16, lines 29-30 of Vaudo) and since it is a goal of Tanizawa to decrease the number of pits, Vaudo's teachings would allow for high quality epitaxial layers with less pits to be grown.

Re claim 53: Tanizawa teaches the LED, wherein the undoped GaN layer (**UDG**) is directly formed on the GaN layer (**GL**).

Re claim 59: Tanizawa teaches the LED wherein the super lattice structure (**6**) is formed using an alkyl source including TMGa and TMIn and a hydride gas including NH_3 and N_2.

Regarding the process limitations recited in claims 59 ("formed using an alkyl source including TMGa and TMIn and a hydride gas including NH_3 and N_2"), these

would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

3. Claims 42, 47-49, 55-57 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanizawa in view of Vaudo.

Re claim 42: Tanizawa teaches a method for manufacturing a light emitting device, the method comprising the steps of: forming a buffer layer (**2**); forming an N-type gallium nitride layer (**5c**) on the buffer layer (**2**); forming a super lattice structure (multi-layered film **6** of $In_kGa_{1-k}N$/ $In_mGa_{1-m}N$ structure, where m<k; e.g. paragraph 64) including InGaN ($In_kGa_{1-k}N$/ $In_mGa_{1-m}N$) on the N-type gallium nitride layer (**5c**), wherein the super lattice structure (**6**) is not doped with an n-type impurity (to enhance crystallinity, both first and second nitride semiconductor layers are preferably undoped; e.g. paragraph 65), wherein the super lattice structure (**6**) including InGaN includes a plurality of first InGaN layers ($In_kGa_{1-k}N$; hereinafter **"FL"**) and a plurality of second InGaN layers ($In_mGa_{1-m}N$; hereinafter **"SL"**), wherein each of the plurality of first InGaN layers (**FL**) has an In composition less than (m<k; e.g. paragraph 64) an In composition of each of the plurality of second InGaN layers (**SL**), and wherein the first InGaN layer

(**FL**) is directly on (as discussed at paragraph 63, the sequence of the layers comprising **6** may be arbitrarily chosen, therefore, the order can be **FL**, **SL**, **FL**, **SL** or **SL**, **FL**, **SL**, **FL**, therefore, the first sequence would result in **FL** being directly on **5c**) the N-type gallium nitride layer (**5c**); forming an active layer (**7**) on the super lattice structure (**6**) and including an InGaN/InGaN structure of a multi-quantum well structure (active layer **7** is a multiple quantum-well structure made from $In_aGa_{1-a}N$; e.g. paragraph 68), wherein the active layer (**7**) is directly on (as discussed at paragraph 63, the sequence of the layers comprising **6** may be arbitrarily chosen, therefore, the order can be **FL**, **SL**, **FL**, **SL** or **SL**, **FL**, **SL**, **FL**, therefore, the first sequence would result in **7** being directly on **SL**) one of the plurality of second InGaN layers (**SL**); and forming a P-type gallium nitride layer (p-type GaN; e.g. paragraph 77) on the active layer (**7**), wherein the super lattice structure including InGaN has a plurality of pits formed thereon (number of pits occurring in each nitride semiconductor layer; e.g. paragraph 64), and wherein the buffer layer (**2**) is grown at a first temperature (400-800˚C; e.g. paragraph 41), wherein the first InGaN layer of the super lattice structure (**6**) including InGaN is grown at a second temperature (1050˚C; e.g. paragraphs 96 and 98) higher than the first temperature (400-800˚C), wherein the second InGaN layer (**SL**) of the super lattice structure (**6**) including InGaN is grown at a third temperature (800˚C; e.g. paragraph 98) higher than the first temperature (400-800˚C; e.g. paragraph 41) and lower than the second temperature (1050˚C; e.g. paragraphs 96 and 98), and wherein the active layer (**7**) is grown at a fourth temperature of 600-800℃ (less than 800˚C since active layer **7** contains a higher amount of indium) and the fourth temperature (less than 800˚C) is

lower than the second temperature (1050°C) and third temperature (800°C; e.g. paragraphs 96 and 98).

Tanizawa is silent as to explicitly teaching wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm.

Vaudo teaches LED structure with reduced number of pits and further teaches and further teaches a non-zero number of the plurality of pits (base GaN has hexagonal pit density of approximately $10^6 cm^{-2}$ and can be reduced to less than 50 pits per cm^2; e.g. column 16, lines 15-17) is 50 or less per area of 5μm x 5μm. Since 25 pits per μm^2 is approximately $2x10^8$ pits per cm^2, Vaudo's pit density of less than 50 pits per cm^2 meets said claim limitation because any subsequent nitride based layer will have the same, if not less, pits than the density of pits at the base GaN layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo in the device of Tanizawa and have a base GaN layer having less than 50 pits per cm2 allowing for a high quality epitaxial growth to be attained (see column 16, lines 29-30 of Vaudo) and since it is a goal of Tanizawa to decrease the number of pits, Vaudo's teachings would allow for high quality epitaxial layers with less pits to be grown.

Re claim 47: Tanizawa teaches the method wherein the super lattice structure (**6** having alternating layers of $In_kGa_{1-k}N$ and $In_mGa_{1-m}N$; e.g. paragraph 64) including InGaN includes an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer (super lattice structure; e.g. paragraph 60).

Re claim 48: Tanizawa teaches the method wherein each layer of the super lattice structure (**6**) including InGaN has a thickness of 1-3000Å (100Å, 70Å; e.g. paragraph 60).

Re claim 49: Tanizawa teaches the device wherein the super lattice structure (**6**) including InGaN has a photoluminescence characteristic of a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below. Since the structure recited in the prior art is substantially identical to that of the claim, claimed properties are presumed to be present. See MPEP 2112.01(i).

Re claim 55: Tanizawa teaches the method, further comprising: forming an undoped GaN layer (**3**) on the buffer layer (**2**) before forming the N-type gallium nitride layer (**5c**).

Re claim 56: Tanizawa teaches the method, wherein the undoped GaN layer (**3**) is grown at a fifth temperature (1050˚C; e.g. paragraph 93) higher than the first temperature (400-800˚C; e.g. paragraph 41), the second temperature (1050˚C; e.g. paragraph 98), the third temperature (800˚C; e.g. paragraphs 96 and 98) and the fourth temperature (less than 800˚C).

Re claim 57: Tanizawa teaches the method, further comprising: forming a plurality of pits (pits appear on the surface of the p-type contact layer **10** are produced from pits formed in layers below it; e.g. paragraph 33 of Tanizawa) between the active layer (**7**) and the P-type gallium nitride layer (**8**).

Re claim 58: Tanizawa teaches the method wherein the step of forming a super lattice structure comprises: forming a super lattice structure (**6**) using an alkyl source

including TMGa and TMIn and a hydride gas including NH_3 and N_2 (TMG, TMI and ammonia are used to form layer **6**; paragraph 98).

Response to Arguments

4. Applicant's arguments with respect to claims 33, 34, 37-42, 44, 47-59 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE Y. MIYOSHI whose telephone number is (571)270-1629. The examiner can normally be reached on M-F 7:30AM-5:00PM EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JYM

/Ori Nadav/
Primary Examiner, Art Unit 2811